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Abstract of the Disclosure

5 A servo loop control apparatus having a master  
microprocessor and at least one autonomous streamlined  
signal processor is disclosed. The architecture provides  
10 a general purpose controller for use in systems where  
intensive servo signal processing is required and is well  
suited to applications where multiple servo control loops  
operate simultaneously. The operation of the streamlined  
signal processors is autonomous from the master processor  
15 so that critical functions can be dedicated to the  
streamlined signal processors. This eliminates complex  
interrupt management and tedious real time scheduling  
constraints, simplifies system design and improves system  
performance. The architecture provides an integrated  
mechanism for implementing multiple, concurrent, complex  
signal processing and embedded control functions, such as  
complete servo-mechanism management for high performance  
disk storage systems.